



ZYWYN CORPORATION

Reliability Qualification Report

ZD1937 Inductor Based Step-Up Converter
For White LED Driver

Date: July 18, 2005

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Revision: 1.0

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Reliability Life Test Result

Life Test

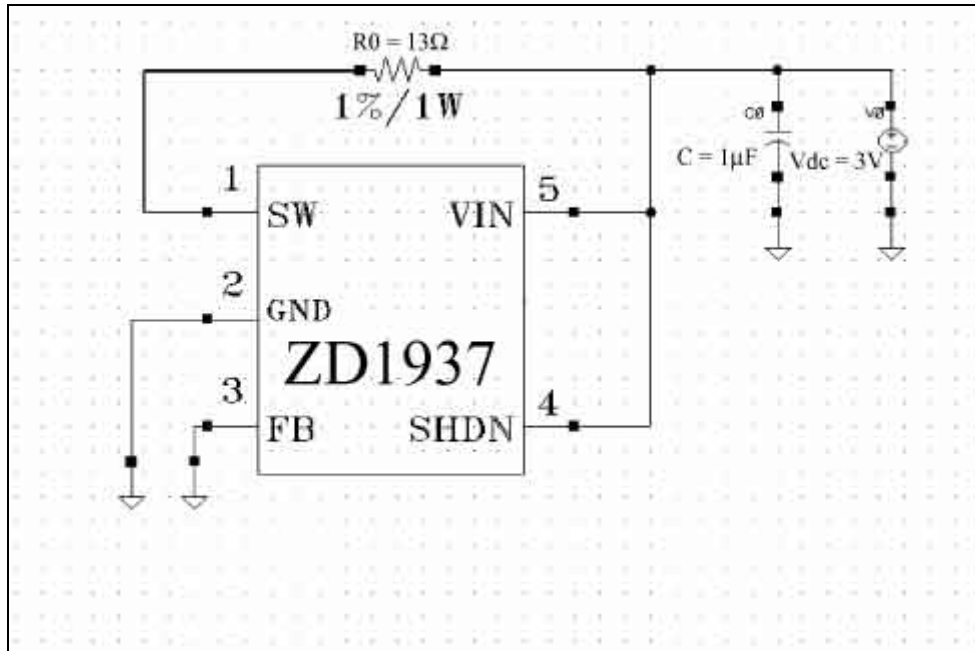
Life Testing is performed to determine if device has any fundamental reliability related failure mechanisms, which can be divided into 4 main groups:

- Process or die related failures, such as oxide-related defects, metallization-related defects and diffusion-related defects.
- Assembly-related defects such as wire bonding or package-related failures.
- Design-related defects.
- Miscellaneous, undetermined or application-induced failures.

Life Test Result

Product Family:	Inductor-Based WLED Driver
Device Type:	ZD1937LB5
Mask Sets:	AP3008
Process:	Bipolar Process
Wafer Manufacturer:	BCD Semiconductor
Package Type:	5-pin SOT23 (Green Package)
Packaging Assemblies:	Jiangsu Changjiang Electronics Technology Co., Ltd., China Lingsen Precision Industries, Ltd., Taiwan
Die Attach Adhesive:	84-1LMISR4
Bond Wire:	1.0 mil HD3
Molding Compound:	EME6710SJ
Lead Finish:	A194/Ag

Burn-In Circuit:



Test Conditions:

- 1) HTOL 168/500/1000 hrs, 3.0V DC, 1.2MHz, 200mA Load, Dynamic Burn-In @125°C
- 2) θ_{JA} of the package (5-pin SOT23) = 256°C/W
- 3) $R_0 = 13\Omega$, 1%/1W; $C_0 = 1\mu F$

Reference Standard:

Mil-Std-883

Pass/Fail Criteria:

Electrical QA testing to datasheet limits at 25°C before and after stress.

Summary:

Device Type	HTOL Test @ 3.0V	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD1937LB5	168 hr	04B27E.5#4	04/29/05	125	80	0
ZD1937LB5	500 hr	04B27E.5#4	04/29/05	125	80	0
ZD1937LB5	1000 hr	04B27E.5#4	04/29/05	125	80	0

FIT Rate Calculation

The FIT (failures in time) is calculated as follows,

$$FR \text{ (Chi-squared)} = \chi^2_{2n+2} / (2 \times AF \times \text{device-hours}) \times 10^9$$

Where, AF is the acceleration factor and n is the number of failures. The value is highly dependent on the following:

1. Life test conditions (duration, temperature, sample size and number of failures)
2. Activation energy of the potential failure modes

The weighted activation energy, E_a , of observed failure mechanisms of Zywyn products has been determined to be 0.7eV.

Based on the above criteria, the FIT rates at 125°C to 55°C, and 150°C to 55°C operation at 60% confidence level, with a sample size of 77 and 1 unit failure allowed, using the BCD Bipolar Process products, have been calculated and listed here below:

+125°C → +55°C			+150°C → +55°C		
Test Time	Failure Rate	Equivalent Life Time	Test Time	Failure Rate	Equivalent Life Time
168 hours	2020 FIT	0.7 year	168 hours	599 FIT	2 years
500 hours	674 FIT	2 years	500 hours	201 FIT	7 years
1000 hours	337 FIT	4 years	1000 hours	100 FIT	14 years
2000 hours	169 FIT	8 years	2000 hours	50 FIT	28 years

1 FIT = 1 failure per billion device hours

Reliability ESD Test Result – Human Body Model

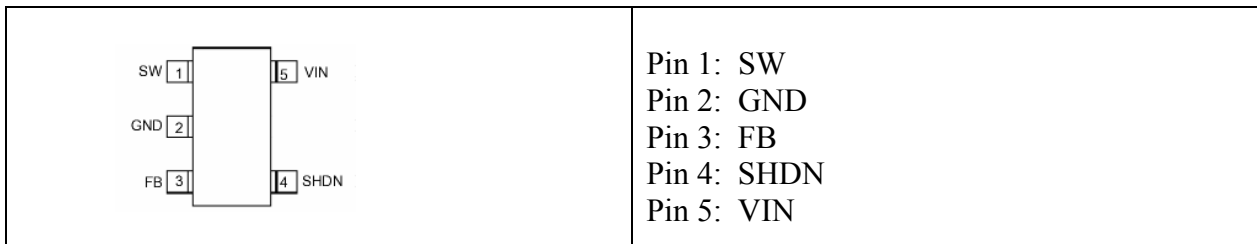
ESD Test Data Input:

Test Vector:	ESD-HBM (Human Body Model)
Reference Standard:	Mil-Std-883E Method 3015.7
Sample Size:	12 units
Test Voltage:	500V~5500V, Step of $\pm 500V$
Pass/Fail Criteria:	Test for Voltage Change at $1\mu A \pm 30\%$
Test Date:	April 20, 2005
Test Equipment:	Keytek Zapmaster 7/4
Test Equipment S/N#:	0008189
Calibration Date:	July 13, 2004
Recommended Next Calibration Due Date:	July 12, 2005
Environmental Condition At Laboratory:	Actual temperature: $+21.6^{\circ}C \sim +21.7^{\circ}C$ Actual humidity: $54\% \sim 55\% RH$

Test Conditions:

SW, FB, SHDN, VIN Pins to GND:	+VE ZAP
SW, FB, SHDN, VIN Pins to GND:	-VE ZAP
SW, GND, FB, SHDN Pins to VCC:	+VE ZAP
SW, GND, FB, SHDN Pins to VCC:	-VE ZAP

ZD1937LB5 Pin Configuration:



Test Results:

Test Model: Human Body Model (HBM)	ESD Sensitivity Passing Target: $\pm 2500\text{V}$	V Class: 2
Pin Combination	Sample Size	Passed Voltage
SW, FB, SHDN, VIN to GND (+)	#1-1 ~ #1-3	+2500V
SW, FB, SHDN, VIN to GND (-)	#2-1 ~ #2-3	-5500V
SW, GND, FB, SHDN to Vcc (+)	#3-1 ~ #3-3	+3000V
SW, GND, FB, SHDN to Vcc (-)	#4-1 ~ #4-3	-3000V
Per Mil-Std-883E-3015.7 Test		
Classification:		
Class 1: 0 volt to 1999 volts		
Class 2: 2000 volts to 3999 volts		
Class 3: 4000 volts and up		

Test Condition: SW, FB, SHDN, VIN to GND (+)				
\ Fail Voltage \ (units:V)		Test Sample#		
Test Pin	Pin Description	#1-1	#1-2	#1-3
1	SW	PASS	PASS	PASS
2	GND	GND	GND	GND
3	FB	PASS	PASS	PASS
4	SHDN	3500	3000	3500
5	VIN	4000	4000	4000

Test Condition: SW, FB, SHDN, VIN to GND (-)				
\ Fail Voltage \ (units:V)		Test Sample#		
Test Pin	Pin Description	#2-1	#2-2	#2-3
1	SW	PASS	PASS	PASS
2	GND	GND	GND	GND
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	PASS	PASS	PASS

Test Condition: SW, GND, FB, SHDN to V_{CC} (+)				
\ Fail Voltage \ (units:V)		Test Sample#		
Test Pin	Pin Description	#3-1	#3-2	#3-3
1	SW	PASS	PASS	PASS
2	GND	PASS	PASS	PASS
3	FB	PASS	PASS	PASS
4	SHDN	3500	4000	4500
5	VIN	VIN	VIN	VIN

Test Condition: SW, GND, FB, SHDN to V_{CC} (-)				
\ Fail Voltage \ (units:V)		Test Sample#		
Test Pin	Pin Description	#4-1	#4-2	#4-3
1	SW	PASS	PASS	PASS
2	GND	4000	3500	3500
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	VIN	VIN	VIN

Reliability ESD Test Result – Machine Model

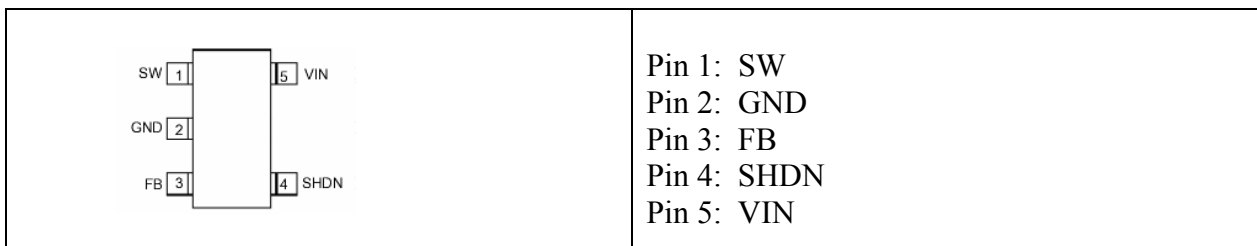
ESD Test Data Input:

Test Vector:	ESD-MM (Machine Model)
Reference Standard:	JEDEC EIA/JESD22-A115
Sample Size:	12 units
Test Voltage:	50V~500V, Step of $\pm 50V$
Pass/Fail Criteria:	Test for Voltage Change at $1\mu A \pm 30\%$
Test Date:	April 20, 2005
Test Equipment:	Keytek Zapmaster 7/4
Test Equipment S/N#:	0008189
Calibration Date:	July 13, 2004
Recommended Next Calibration Due Date:	July 12, 2005
Environmental Condition At Laboratory:	Actual temperature: $+21.6^{\circ}C \sim +21.7^{\circ}C$ Actual humidity: $54\% \sim 55\% RH$

Test Conditions:

SW, FB, SHDN, VIN Pins to GND:	+VE ZAP
SW, FB, SHDN, VIN Pins to GND:	-VE ZAP
SW, GND, FB, SHDN Pins to VCC:	+VE ZAP
SW, GND, FB, SHDN Pins to VCC:	-VE ZAP

ZD1937LB5 Pin Configuration:



Test Results:

Test Model: Machine Model (MM)		ESD Sensitivity Passing Target: $\pm 350V$		V Class: B
Pin Combination		Sample Size	Passed Voltage	Per JEDEC EIA/JESD22-A115 Test
SW, FB, SHDN, VIN to GND (+)		#M1-1 ~ #M1-3	+350V	Classification: Class A: 0 volt to 199 volts Class B: 200 volts to 399 volts Class C: 400 volts and up
SW, FB, SHDN, VIN to GND (-)		#M2-1 ~ #M2-3	-500V	
SW, GND, FB, SHDN to Vcc (+)		#M3-1 ~ #M3-3	+400V	
SW, GND, FB, SHDN to Vcc (-)		#M4-1 ~ #M4-3	-500V	

Test Condition: SW, FB, SHDN, VIN to GND (+)				
\\ Fail Voltage \\ (units:V)		Test Sample#		
Test Pin	Pin Description	#M1-1	#M1-2	#M1-3
1	SW	PASS	PASS	PASS
2	GND	GND	GND	GND
3	FB	PASS	PASS	PASS
4	SHDN	500	400	PASS
5	VIN	PASS	PASS	PASS

Test Condition: SW, FB, SHDN, VIN to GND (-)				
\\ Fail Voltage \\ (units:V)		Test Sample#		
Test Pin	Pin Description	#M2-1	#M2-2	#M2-3
1	SW	PASS	PASS	PASS
2	GND	GND	GND	GND
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	PASS	PASS	PASS

Test Condition: SW, GND, FB, SHDN to V _{CC} (+)				
\\ Fail Voltage \\ (units:V)		Test Sample#		
Test Pin	Pin Description	#M3-1	#M3-2	#M3-3
1	SW	PASS	PASS	PASS
2	GND	PASS	PASS	PASS
3	FB	PASS	PASS	PASS
4	SHDN	PASS	450	500
5	VIN	VIN	VIN	VIN

Test Condition: SW, GND, FB, SHDN to V _{CC} (-)				
\\ Fail Voltage \\ (units:V)		Test Sample#		
Test Pin	Pin Description	#M4-1	#M4-2	#M4-3
1	SW	PASS	PASS	PASS
2	GND	PASS	PASS	PASS
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	VIN	VIN	VIN

Reliability ESD Test Result – Latch-Up Test

ESD Test Data Input:

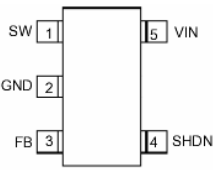
Test Vector: ESD/Latch-Up
Reference Standard: JEDEC Standard No. 78, August 1997
Sample Size: 9 units
Test Voltage: Positive Current Trigger, +25mA~+200mA,
+25mA Step (+);
Negative Current Trigger, -25mA~-200mA,
-25mA Step (-);
V Supply Over-Voltage Test, +15V~+23V,
+1V Step (+)
Pass/Fail Criteria: <25mA, 10mA+I_{normal}; >25mA, 1.4xI_{normal}
Test Date: April 20, 2005

Test Equipment: Keytek Zapmaster 7/4
Test Equipment S/N#: 0008189
Calibration Date: July 13, 2004
Recommended Next
Calibration Due Date: July 12, 2005
Environmental Condition At Laboratory: Actual temperature: +22.3°C ~ +22.5°C
Actual humidity: 45% ~ 47% RH

Test Conditions:

Positive Current I
Negative Current I
V_{supply} OVER-VOLTAGE Test

ZD1937LB5 Pin Configuration:

	<p>Pin 1: SW Pin 2: GND Pin 3: FB Pin 4: SHDN Pin 5: VIN</p> <p>I/O: SW I/P: FB, SHDN VCC: VIN GND: GND</p>
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Test Results:

Test Model: ESD/Latch-Up Trigger Model	Tested Pins	Sample Size	Trigger Source Induced Latch-Up	IT Class: 3 Per JEDEC Std. #78, Aug. 1997 Test
+IT	I/P	3	+200mA	Class1: +IT: 0 mA ~ +39 mA -IT: 0 mA ~ -39 mA
	I/O		+200mA	
-IT	I/P	3	-200mA	Class2: +IT: +40 mA ~ +99 mA -IT: -40 mA ~ -99 mA
	I/O		-200mA	
Vsupply Over-Voltage Test	VCC	3	23.0V	Class3: +IT: +100 mA and up -IT: -100 mA and below

Test Condition: Positive Current I				
\ TrIGGERED Current \ (units:mA)		Tested Sample#		
Test Pin	Pin Description	#1	#2	#3
1	SW	PASS	PASS	PASS
2	GND	VSS	VSS	VSS
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	VIN	VIN	VIN

Test Condition: Negative Current I				
\ TrIGGERED Current \ (units:mA)		Tested Sample#		
Test Pin	Pin Description	#4	#5	#6
1	SW	PASS	PASS	PASS
2	GND	VSS	VSS	VSS
3	FB	PASS	PASS	PASS
4	SHDN	PASS	PASS	PASS
5	VIN	VIN	VIN	VIN

Test Condition: Vsupply OVER-VOLTAGE Test				
\ TrIGGERED Voltage \ (units:V)		Tested Sample#		
Test Pin	Pin Description	#7	#8	#9
2	GND	VSS	VSS	VSS
5	VIN	PASS	PASS	PASS

Remarks:

- 1) The Ground Pin was not tested for Latch-Up.
- 2) The positive or negative current pulse (I-Test) or voltage pulse (Vsupply Over-Voltage Test) was applied to any pin under test in an attempt to induce a latch-up.
- 3) The data report only applies to the specimen samples submitted for this test and is considered invalid if used separately in other measures.