



ZYWYN CORPORATION

Reliability Qualification Report

ZD1680

High Efficiency Step-Up 6-Channels LED Controller

Date: April 9, 2010

Revision: 1.0

<u>Table of Contents</u>	<u>Page</u>
Life Test	3
Fit Rate Calculation	5
ESD Test	6
Temp Cycle Test	7
Appendix I	
5x5 32-Pin Exposed Pad QFN Reliability Report	8~17
Appendix II	
28-Pin Exposed Pad TSSOP Reliability Report	18~29
Appendix III	
Photos of Test Equipment	30~31
Appendix IV	
ESD Test Sequence	32

Reliability Life Test Result

Life Test

Life Testing is performed to determine if device has any fundamental reliability related failure mechanisms, which can be divided into 4 main groups:

- Process or die related failures, such as oxide-related defects, metallization-related defects and diffusion-related defects.
- Assembly-related defects such as wire bonding or package-related failures.
- Design-related defects.
- Miscellaneous, undetermined or application-induced failures.

Life Test Result

Product Family:	High Efficiency Step-Up 6-Channel LED Controller
Device Type:	ZD1680
Mask Sets:	MS199B
Processes:	Episil 0.5 μ m 2 Poly-2Metal 40V BCD Process
Wafer Manufacturer:	Episil Technologies, Inc.
Package Type:	28-Pin Exposed Pad TSSOP, 5X5 32-Pin Exposed Pad QFN
Package Manufacturer:	GREATEK ELECTRONICS IN Taiwan
Die Attach Adhesive:	CRM-1033BF
Bond Wire:	Gold wire 1.2 mil
Test:	Refer to Reliability Test Results in GREATEK ELECTRONICS Reliability report
Reference Standard:	Mil-Std-883
Pass/Fail Criteria:	Electrical QA testing to datasheet limits at 25°C before and after stress.

Summary:

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD1680LEY	500 hr	C8B05D55.1	01/06/2010	100	10	0
ZD1680LEY	1000 hr	C8B05D55.1	01/27/2010	100	10	0

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD1680LEY	500 hr	C8B05D55.1	05/27/2009	100	10	0
ZD1680LEY	1000 hr	C8B05D55.1	06/17/2009	100	10	0

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD1680LEY	500 hr	C8A14A53.1	03/13/2008	100	25	0
ZD1680LEY	1000 hr	C8A14A53.1	04/03/2008	100	25	0

FIT Rate Calculation

The FIT (failures in time) is calculated as follows,

$$\text{FR (Chi-squared)} = \chi^2_{2n+2} / (2 \times \text{AF} \times \text{device-hours}) \times 10^9$$

where AF is the acceleration factor and n is the number of failures. The value is highly dependent on the following:

1. Life test conditions (duration, temperature, sample size and number of failures)
2. Activation energy of the potential failure modes

The weighted activation energy, E_a , of observed failure mechanisms of Zywyn products has been determined to be 0.8eV.

Based on the above criteria, the FIT rates at 25°C, 55°C, and 75°C operation at both 60% and 90% confidence levels for the ZD1680 using Episil 0.5µm 2 Poly-2Metal 40V BCD Process have been calculated and are listed below.

Device Type	Confidence Level	+25°C	+55°C	+75°C
ZD1680LEY	60%	39.45	676.02	3423.16
ZD1680LEY	90%	99.14	1698.8	8602.2

1 FIT = 1 failure per billion device hours

ESD Test Results

ZD1680 devices were submitted for Human Body Model ESD test.

Summary:

Device Type	ESD Test	Lot Number	Date Completed	Sample Size	No. of Fails
ZD1680LEY	±2000V HBM	C8A14A53.1	6/26/2009	6	0

Device Type	ESD Test	Lot Number	Date Completed	Sample Size	No. of Fails
ZD1680LEY	±2000V HBM	C8B05D55.1	6/26/2009	6	0

Temp Cycle Test Result

Zywyn's High Efficiency Step-Up 6-Channel LED Controller products are packaged in a 5X5 32-Pin Exposed Pad QFN and 28-Pin Exposed Pad TSSOP Green Package. Packaged Qualification Reliability Report which consists of, among others, Temp Cycle Test from vendors, is attached for reference. The report shows the devices pass the test with no failure.

Appendix I

5X5 32-PIN QFN Reliability Report



GREATEK ELECTRONICS INC.

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Tel : (037)638-568 Fax : (037)628-323

Reliability Test Report

Customer : ***

Purpose : Reliability Test.

Package Type : QFN 32L (5*5)

Report No : B510-RELI-0906121

Report Date :07-AUG-2009

Conclusion : The test results were all passed

Approved By: STEVEN SL Prepared By: Wanda Wei

Date : 07-AUG-2009

Date : 07-AUG-2009

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1. Sample Background

1.1 Sample Background:

Package Type :	QFN 32L (5*5)	L/F Material :	A194
Device :	*	Lead Frame:	134*134 (mil)
Lot No:	*	Silver Epoxy:	1076DJ-G
Mo No:	XNA532494270	Gold Wire:	0.9mil
Coating :	NO	Compound	G700H
Exposed pad :	YES	Lead Finish	Pure Tin
Apply Date:	02-JUN-2009	Sample Size:	180EA
Complete Date:	31-JUL-2009	Report No:	B510-RELI-0906121



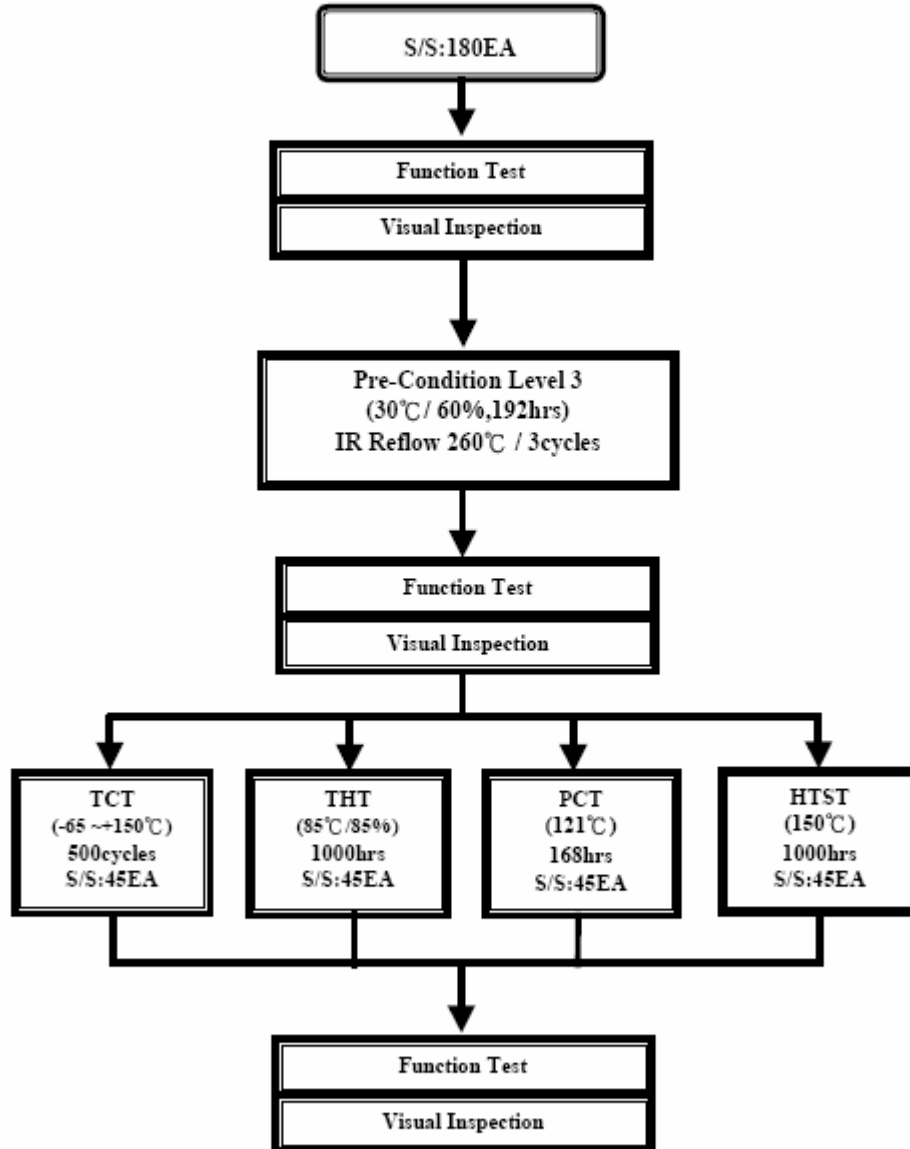
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2. Test Flow Chart

2.1 Precondition:





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3. Inspection method

3.1 Visual Inspection:

Purpose: In order to check whether the samples have package crack or not before/after reliability test.

Apparatus: Power Scope (7~40x)

3.2 SAT Inspection:

Purpose: Inspecting the delamination of concerned layer.

Apparatus: SONIX FUSION

4. Environment Stress / Mechanical Test

4.1 Precondition:

This test method establishes an industry standard preconditioning flow for plastic SMDs (surface mount device) that is representative of a typical industry multiple solder reflow operation.

Test procedure is as following:

Stept1: TCT 5cycles

Stept2: Bake 125°C ,24hrs

Stept3: Moisture Soak (30°C/60%/192hrs)

Stept4: IR Reflow 260°C / 3cycles

4.2 PCT:

The "Accelerated Moisture Resistance Test" is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged solid state devices. It employs severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. This test is destructive; it may* be used for qualification, lot acceptance and as a product monitor.

Test condition: 121°C, 2atm, 168hrs.

4.3 TCT:

This test is conducted to determine the resistance of a part to extremes of high- and low-temperatures, and to the effect of alternate exposures to these extremes.

Test condition: -65°C ~ +150°C, 500cycles.

4.4 HTST:

The purpose of this test is to determine the effect on solid state electronic devices of storage at elevated temperature without electrical stress applied. This test is considered destructive and, therefore, is applicable for device qualification.

Test condition: 150°C, 1000hrs



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4.5 THT(egual to THB without bias):

The Steady-State Temperature Humidity Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs conditions of temperature and humidity which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Test condition: 85°C/85% ,1000hrs



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5. Reliability Test Results

5.1 Summary of test results:

Test Procedure	Sample Size	Visual Insp. Rej/s.s	Function Test rej/s.s	SAT insp Rej/s.s	Judgment
Before Pre-condition	180EA	0/180	0/180	0/45	PASS
After Pre-condition	180EA	0/180	0/180	0/45	PASS
PCT 168hrs	45EA	0/45	0/45	N/A	PASS
THT 1000hrs	45EA	0/45	0/45	N/A	PASS
HTST 1000hrs	45EA	0/45	0/45	N/A	PASS
TCT 500cycles	45EA	0/45	0/45	N/A	PASS

5.2 Detail Informations of SAT Inspection :

Focus	Die Surface (Top)				Die Pad(back side)			
	0% acc	0%~10% rej	>10% rej	SAT Photo	0% acc	0%~50% acc	>50% rej	SAT Photo
Before Precondition	45	0	0	Fig 1	Exposed pad			
After Precondition	45	0	0	Fig 2	Exposed pad			

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6. Conclusion

6.1 The test results were all passed.

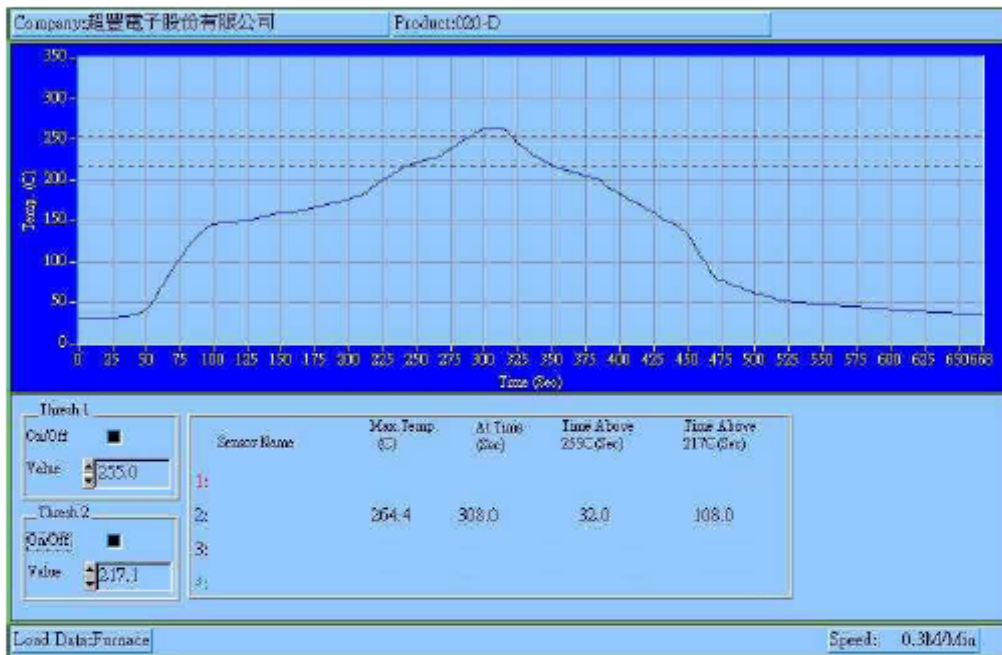
7. Reference

- * JESD22-A113 Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing
- * IPC / JEDEC J-STD-020D IR Reflow
- * Greatek Spec #QA-00-300 Reliability Test Instruction
- * Greatek Spec #QA-00-301 Pressure Cooker Test
- * Greatek Spec #QA-00-302 Temperature/Humidity Chamber Operation Instruction
- * Greatek Spec #QA-00-303 IR Reflow Test System Operation Instruction
- * Greatek Spec #QA-00-305 Temperature cycling
- * Greatek Spec #QA-00-402 SAT Operation Instruction



8. Attachments:

IR PROFILE(Tmax:260°C) for SMD.



Condition	Spec.	Actual
Time above 217°C	60-150 seconds.	108 seconds.
Peak Temperature	>260°C	264.4°C
Time within 5°C of actual peak temperature	>30 seconds.	32 seconds.



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9. SAT Photo :

9.1 Before / After Precondition :



Package Type: QFN 32L (5*5)
Before Pre-con LEVEL 3
Photo no : Fig 1
Die Surface SAT Result : 0/45ea delam =>PASS.



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Package Type: QFN 32L (5*5)
After Pre-con LEVEL 3
Photo no : Fig 2
Die Surface SAT Result : 0/45ea dalam =>PASS.

Appendix II

28-PIN TSSOP Reliability Report



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Tel : (037)638-568 Fax : (037)628-323

Reliability Test Report

Customer : ***

Purpose : Reliability Test

Package Type : TSSOP 28L (173mil)

Report No : B510-RELI-0906004

Report Date :01-FEB-2010

Conclusion : The test results were all passed

Approved By: SEAN SU

Prepared By : Wanda Wei

Date : 01-FEB-2010

Date : 01-FEB2010

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1. Sample Background

1.1 Sample Background:

Package Type :	TSSOP 28L (173mil)	L/F Material :	C7025
Device :	*	Lead Frame:	105*140 (mil)
Lot No:	*	Silver Epoxy:	1076DJ-G
Mo No:	UNA28U593924E	Gold Wire:	1.0mil
Coating :	NO	Compound	G600F
Exposed pad :	YES	Lead Finish	Pure Tin
Apply Date:	03-JUN-2009	Sample Size:	92EA
Complete Date:	26-JAN-2010	Report No:	B510-RELI-0906004

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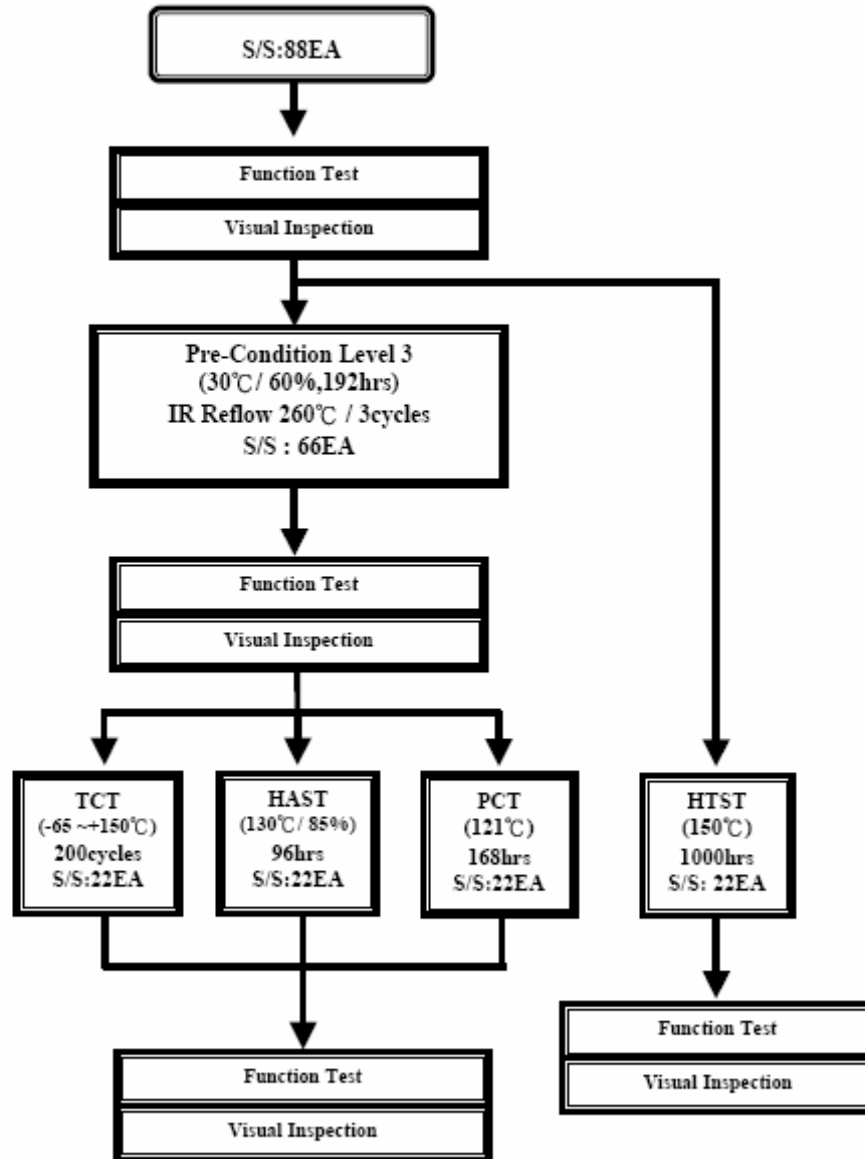
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2. Test Flow Chart

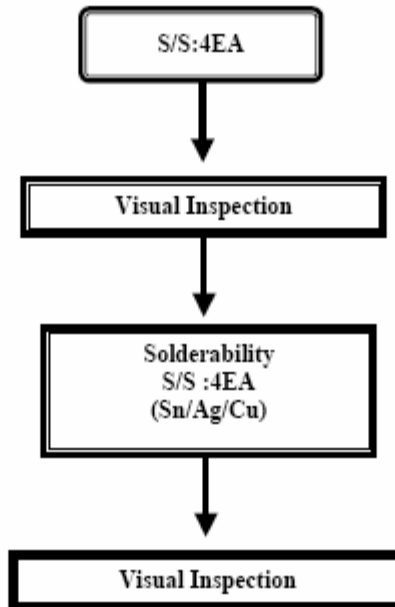
2.1 Precondition:



2



2.2 Solderability :





3. Inspection method

3.1 Visual Inspection:

Purpose: In order to check whether the samples have package crack or not before/after reliability test.

Apparatus: Power Scope (7~40x)

3.2 SAT Inspection:

Purpose: Inspecting the delamination of concerned layer.

Apparatus: SONIX FUSION

4. Environment Stress / Mechanical Test

4.1 Precondition:

This test method establishes an industry standard preconditioning flow for plastic SMDs (surface mount device) that is representative of a typical industry multiple solder reflow operation.

Test procedure is as following:

Step1: TCT 5cycles

Step2: Bake 125°C ,24hrs

Step3: Moisture Soak (30°C/60%/192hrs)

Step4: IR Reflow 260°C / 3cycles

4.2 Pressure Cooker Test :

The "Accelerated Moisture Resistance Test" is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged solid state devices. It employs severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. This test is destructive; it may* be used for qualification, lot acceptance and as a product monitor.

Test condition: 121°C, 2atm, 168hrs.

4.3 Temperature Cycle Test :

This test is conducted to determine the resistance of a part to extremes of high- and low-temperatures, and to the effect of alternate exposures to these extremes.

Test condition: -65°C ~ +150°C, 200cycles.

4.4 High Temperature Storage Life:

The purpose of this test is to determine the effect on solid state electronic devices of storage at elevated temperature without electrical stress applied. This test is considered destructive and, therefore, is applicable for device qualification.

Test condition: 150°C, 1000hrs



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4.5 Highly Acceleration Life :

The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test .
(JEDEC Standard No. 22-A101).

Test condition: 130°C/85% , 96 hrs.

4.6 Solderability:

The purpose of this test method is to evaluation the solderability of terminations that are normally joined by soldering operation. This evaluation is made on the basis of the ability of these terminations be wetted by a coating of solder ,and to produce a suitable fillet when dip soldered.

Test procedure is as following:

Step1: Steam aging (8hrs)

Step2: Dipping with flux(type R) , Condition: 245±5°C , Dwell Time:5±0.5secs.

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5. Reliability Test Results

5.1 Summary of test results :

Test Procedure	Sample Size	Visual Insp. Rej/s.s	Function Test rej/s.s	SAT insp Rej/s.s	Judgment
Before Pre-condition	66EA	0/66	0/66	0/66	PASS
After Pre-condition	66EA	0/66	0/66	0/66	PASS
HTST 1000hrs	22EA	0/22	0/22	N/A	PASS
PCT 168hrs	22EA	0/22	0/22	N/A	PASS
HAST 96hrs	22EA	0/22	0/22	N/A	PASS
TCT 200cycles	22EA	0/22	0/22	N/A	PASS
Solderability	4EA	0/4	N/A	N/A	PASS

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5.2 Detail Informations of SAT Inspection :

5.2-1 Before Precondition :

Focus	Die Surface				L/F Surface			
spec	0% acc	0%~10% rej	>10% rej	SAT Photo	0% acc	Partial length on lead	Entire length on lead	SAT Photo
Before Pre-condition	22	0	0	Fig1	22	0	0	Fig1
Focus	Die Pad(Top side) <No Ground Bond>				Die Pad(back side)			
spec	0%	0%~10%	>10%	SAT Photo	0% acc	0%~50% acc	>50% rej	SAT Photo
Before Pre-condition	22	0	0	Fig1	Exposed pad			

5.2-2 After Precondition :

Focus	Die Surface				L/F Surface			
spec	0% acc	0%~10% rej	>10% rej	SAT Photo	0% acc	Partial length on lead	Entire length on lead	SAT Photo
After Pre-condition	22	0	0	Fig2	21	1	0	Fig2
Focus	Die Pad(Top side) <No Ground Bond>				Die Pad(back side)			
spec	0%	0%~10%	>10%	SAT Photo	0% acc	0%~50% acc	>50% rej	SAT Photo
After Pre-condition	22	0	0	Fig2	Exposed pad			

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6. Conclusion

6.1 The test results were all passed.

7. Reference

- * JESD22-A113 Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing
- * IPC / JEDEC J-STD-020D IR Reflow
- * Greatek Spec #QA-00-300 Reliability Test Instruction
- * Greatek Spec #QA-00-301 Pressure Cooker Test
- * Greatek Spec #QA-00-302 Temperature/Humidity Chamber Operation Instruction
- * Greatek Spec #QA-00-303 IR Reflow Test System Operation Instruction
- * Greatek Spec #QA-00-304 Solderability Test Operation Instruction
- * Greatek Spec #QA-00-305 Temperature cycling
- * Greatek Spec #QA-00-306 Highly Acceleration Life
- * Greatek Spec #QA-00-402 SAT Operation Instruction

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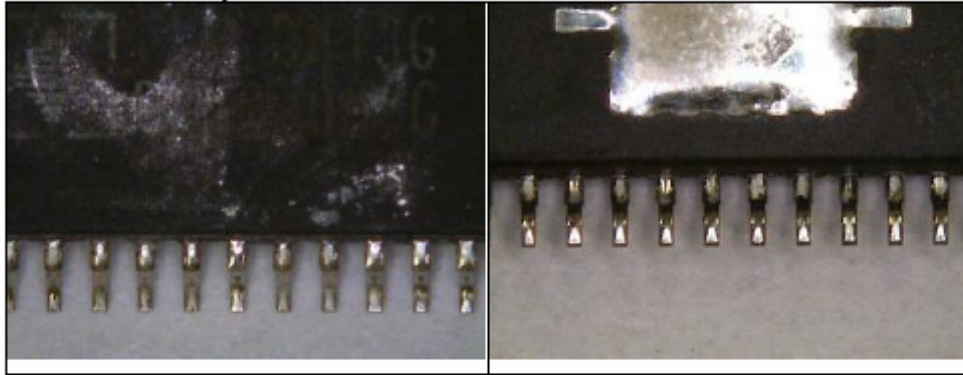
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8. Solder Picture:

8.1 After solderability :

Top side

Back side



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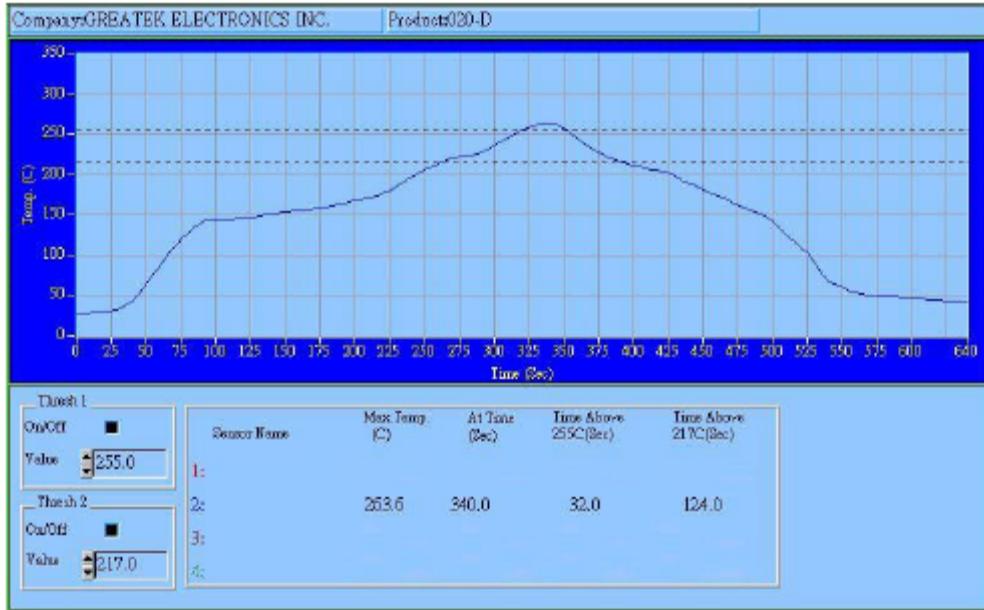
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9. Attachments:

IR PROFILE(Tmax:260°C) for SMD.



Condition	Spec.	Actual
Time above 217°C	60-150 seconds.	124 seconds.
Peak Temperature	>260°C	263.6°C
Time within 5°C of actual peak temperature	>30 seconds.	32 seconds.

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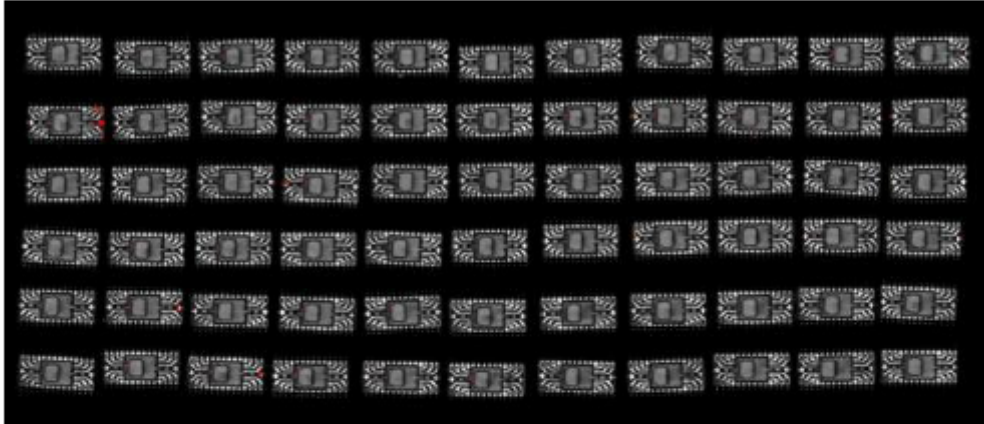
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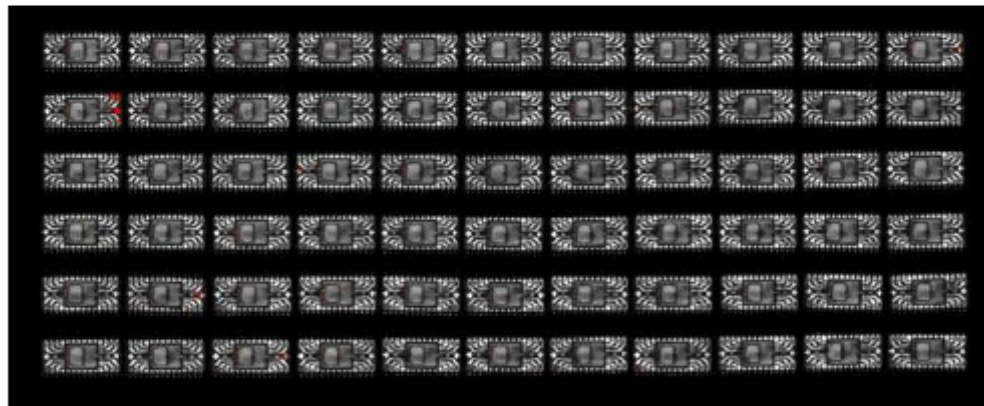


10. SAT Photo :

10.1 Before / After Precondition :



Package Type:TSSOP 28L (173mil)
Before Pre-con LEVEL 3
Photo no : Fig 1
Die Surface SAT Result : 0/66ea dalam =>PASS

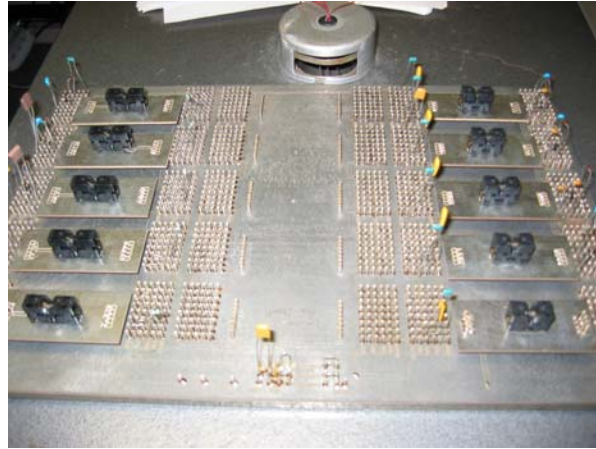


Package Type: TSSOP 28L (173mil)
After Pre-con LEVEL 3
Photo no : Fig 2
Die Surface SAT Result : 0/66ea dalam =>PASS.

Appendix III

Testing Equipment

Burn-in board and burn-in equipment



Burn-in Board used for testing



Burn-in oven used for testing

ESD Testing Equipment



Front view of the iMCS model #700



Front view of the iMCS model #700 with lid open

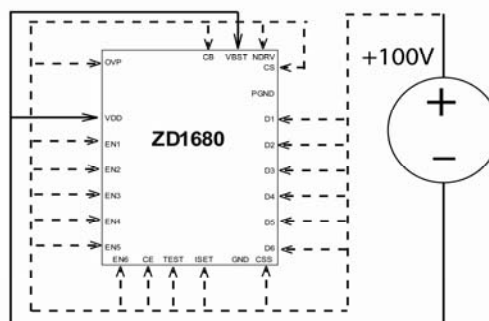


Back view of the ESD Tester with the Machine Model/Pulse Model being used

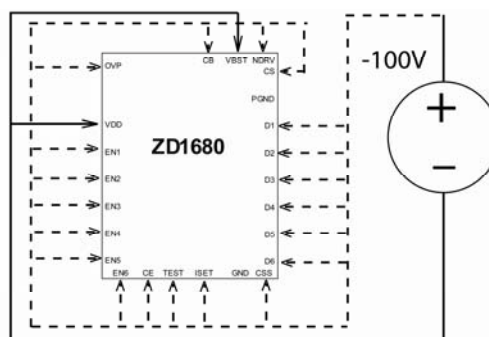
Appendix IV

ESD Test Sequence for 5x5 32-Pin EP QFN & 28-Pin EP TSSOP

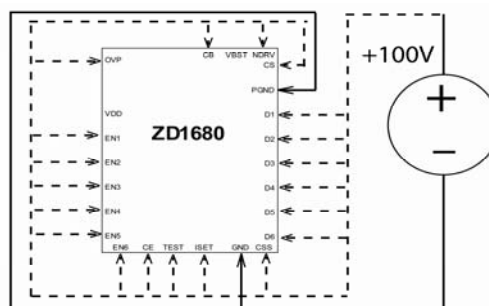
Step 1. Connect VIN to ground and apply +100V to each pin, one at a time.



Step 2. Repeat Step 1 using -100V.



Step 3. Connect GND to ground and apply +100V to each pin, one at a time.



Step 4. Repeat Step 3 using -100V.
Step 5. Check DUT for damage.
Step 6. If DUT is undamaged, repeat Steps 1-5 for two additional units.
Step 7. When three units pass sequence, repeat Steps 1-6 for three additional parts and increase voltage by |100|V until |2000|V is reached and passed

