ZYWYN CORPORATION

Reliability Qualification Report

ZD850 High Power AC/DC or DC/DC LED Display Driver

Date: August 18, 2008
Revision: 1.0

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Reliability Life Test Result

Life Test

Life Testing is performed to determine if device has any fundamental reliability related failure mechanisms, which can be divided into 4 main groups:

- Process or die related failures, such as oxide-related defects, metallization-related defects and diffusion-related defects.
- Assembly-related defects such as wire bonding or package-related failures.
- Design-related defects.
- Miscellaneous, undetermined or application-induced failures.

Life Test Result

Product Family:	High Power AC/DC or DC/DC LED Display Driver
Device Type:	ZD850
Mask Sets:	MS184A
Processes:	Episil 0.5µm 2 Poly-2Metal 40V BCD Process
Wafer Manufacturer:	Episil Technologies, Inc.
Package Type:	16-Pin Exposed TSSOP
Package Manufacturer:	Greatek Electronics INC. in Taiwan
Die Attach Adhesive:	CRM-1033BF
Bond Wire:	Gold wire 1.2 mil
Test:	Refer to Reliability Test Results in Greatek's Reliability report
Reference Standard:	Mil-Std-883
Pass/Fail Criteria:	Electrical QA testing to datasheet limits at 25°C before and after stress.

Summary:

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD850LEY	500 hr @ 12VAC	716973.1	02/29/2008	100	5	0
ZD850LEY	1000 hr @ 12VAC	716973.1	03/21/2008	100	5	0

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD850LEY	500 hr @ 12VAC	799097.1	02/29/2008	100	5	0
ZD850LEY	1000 hr @ 12VAC	799097.1	03/21/2008	100	5	0

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD850LEY	500 hr @ 12VDC	799097.1	07/28/2008	100	5	0
ZD850LEY	1000 hr @ 12VDC	799097.1	08/18/2008	100	5	0

FIT Rate Calculation

The FIT (failures in time) is the calculated as follows,

$$FR\ (\text{Chi-squared}) = \chi^2_{2n+2} / (2 \times AF \times \text{device-hours}) \times 10^9$$

where AF is the acceleration factor and n is the number of failures. The value is highly dependent on the following:

1. Life test conditions (duration, temperature, sample size and number of failures)
2. Activation energy of the potential failure modes

The weighted activation energy, Ea, of observed failure mechanisms of Zywyn products has been determined to be 0.8eV.

Based on the above criteria, the FIT rates at 25°C, 55°C, and 75°C operation at both 60% and 90% confidence levels for the ZD850 using Episil 0.5µm 2 Poly-2Metal 40V BCD Process have been calculated and are listed below.

Device Type	Confidence Level	+25°C	+55°C	+75°C
ZD850	60%	118.35	2028.06	10269.4
ZD850	90%	297.41	5096.39	25806.5

1 FIT = 1 failure per billion device hours

ESD Test Results

ZD850 devices were submitted for Human Body Model ESD test.

Summary:

Device Type	ESD Test	Lot Number	Date Completed	Sample Size	No. of Fails
ZD850LEY	±1000V HBM	716973.1	10/1/2007	6	0

Device Type	ESD Test	Lot Number	Date Completed	Sample Size	No. of Fails
ZD850LEY	±1000V HBM	799097.1	01/25/2008	6	0

Temp Cycle Test Result

Zywyn's High Power AC/DC or DC/DC LED Display driver products are packaged in a 16-Pin Exposed TSSOP Green Package. Packaged Qualification Reliability Report which consists of, among others, Temp Cycle Test from vendors, is attached for reference. The report shows the devices pass the test with no failure.

Appendix I

16-PIN Exposed TSSOP Reliability Report

GREATEK ELECTRONICS INC.
No.136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien Taiwan R.O.C.
Tel : (037)638-568 Fax : (037)628-323

Reliability Test Report

Customer : ***
Purpose : Reliability test
Package Type : TSSOP 16L
Report No : B510--RELI-0611027
Report Date :16-FEB-2007
Conclusion : The test results were all passed

Approved By: Steven Su Prepared By : Wanda Wei

Date : 16-FEB-2007 Date : 16-FEB-2007

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GREATEK ELECTRONICS INC.
No.136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien Taiwan R.O.C.
Tel : (037)638-568 Fax : (037)628-323

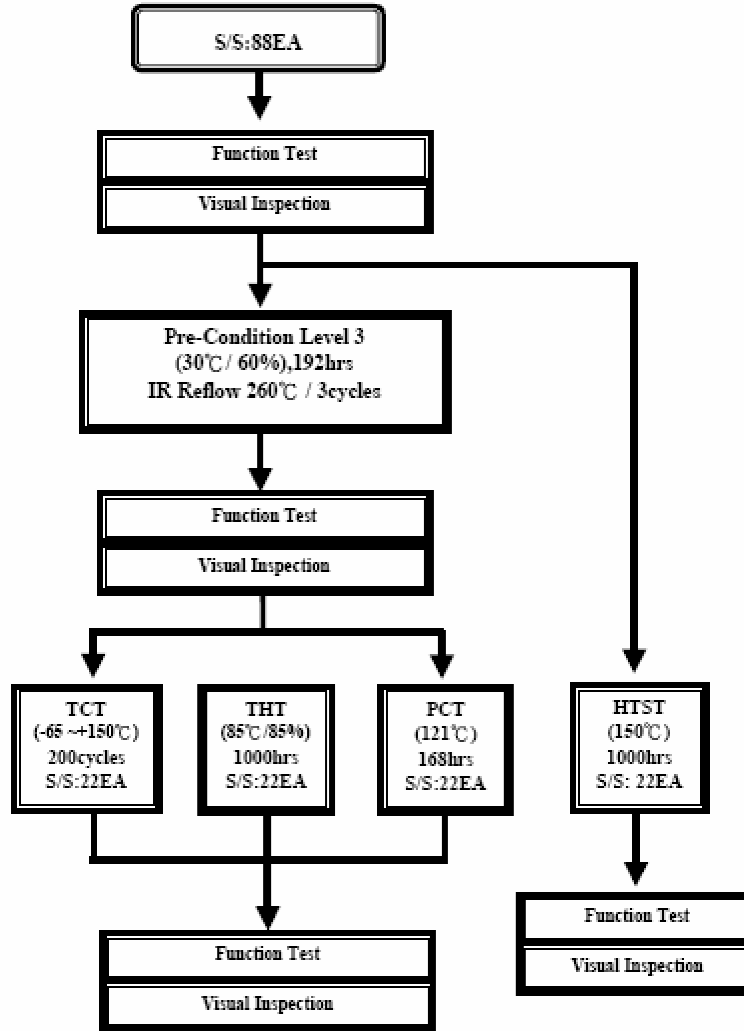
1. Sample Background

1.1 Sample Background:

Package Type :	TSSOP 16L	Lead Frame:	118*11E (mil)
Device :	*	Silver Epoxy:	8352L
Lot No:	*	Gold Wire:	1.0mil
Mo No:	UBF16UA63453	Compound	G600F
Coating :	NO	Lead Finish	Pure Tin
Apply Date:	22-NOV-2006	Sample Size:	92EA
Complete Date:	25-JAN-2007	Report No:	B510-RELI-0611031

2. Test Flow Chart

2.1 Precondition:



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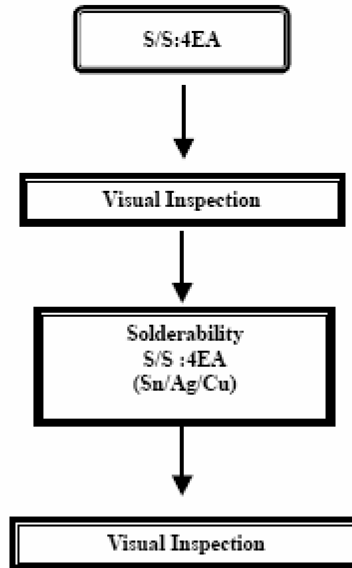
2.2 Solderability:



3. Inspection method

3.1 Visual Inspection:

Purpose: In order to check whether the samples have package crack or not before/after reliability test.

Apparatus: Power Scope (7~40x)

3.2 SAT Inspection:

Purpose: Inspecting the delamination of concerned layer.

Apparatus: SONIX QUANTUM-350

4. Environment Stress / Mechanical Test

4.1 Precondition:

This test method establishes an industry standard preconditioning flow for plastic SMDs (surface mount device) that is representative of a typical industry multiple solder reflow operation.

Test procedure is as following:

Stept1: TCT 5cycles

Stept2: Bake 125℃ ,24hrs

Stept3: Moisture Soak (30℃/60%/192hrs)

Stept4: IR Reflow 260℃ / 3cycles

4.2 PCT:

The "Accelerated Moisture Resistance Test" is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged solid state devices. It employs severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. This test is destructive; it may* be used for qualification, lot acceptance and as a product monitor.

Test condition: 121℃, 2atm, 168hrs.

4.3 TCT:

This test is conducted to determine the resistance of a part to extremes of high- and low-temperatures, and to the effect of alternate exposures to these extremes.

Test condition: -65℃ ~ 150℃,200cycles.

4.4 HTST:

The purpose of this test is to determine the effect on solid state electronic devices of storage at elevated temperature without electrical stress applied. This test is considered destructive and, therefore, is applicable for device qualification.

Test condition: 150℃, 1000hrs

4.5 THT(egual to THB without bias):

The Steady-State Temperature Humidity Test is peformed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs conditions of temperature and humidity which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the inteface between the external protective material and the metallic conductors which pass through it.

Test condition: 85℃/85%,1000hrs

4.6 Solderability:

The purpose of this test method is to evaluation the solderability of terminations that are normally joined by soldering operation. This evaluation is made on the basis of the ability of these terminations be wetted by a coating of solder ,and to produce a suitable fillet when dip soldered.

Test procedure is as following:

Stept1: Steam aging (8hrs)

Stept2: Dipping with flux(type R) , Condition: 245±5℃ , Dwell Time:5±0.5secs.

5. Reliability Test Results

5.1 Summary of test results:

Test Procedure	Sample Size	Visual Insp. Rej/s.s	Function Test rej/s.s	SAT insp Rej/s.s	Judgment
Before Pre-condition	66EA	0/66	0/66	0/66	PASS
After Pre-condition	66EA	0/66	0/66	0/66	PASS
HTST 1000hrs	22EA	0/22	0/22	N/A	PASS
PCT 168hrs	22EA	0/22	0/22	N/A	PASS
THT 1000hrs	22EA	0/22	0/22	N/A	PASS
TCT 200cycles	22EA	0/22	0/22	N/A	PASS
Solderability	4EA	0/4	N/A	N/A	PASS

5.2 Detail Informations of SAT Inspection :

Focus	Die Surface (Top)				Die Pad(back side)			
spec	0% acc	0%~10% rej	>10% rej	SAT Photo	0%	0%~50% acc	>50% rej	SAT Photo
Before Precondition	66	0	0	Fig-1	Exposed pad			
After Precondition	66	0	0	Fig-2	Exposed pad			

6. Conclusion

6.1 The test results were all passed.

7. Reference

- **JESD22-A113** Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing
- **Greatek Spec #QA-00-300** Reliability Test Instruction
- **Greatek Spec #QA-00-301** Pressure Cooker Test
- **Greatek Spec #QA-00-302** Temperature/Humidity Chamber Operation Instruction
- **Greatek Spec #QA-00-303** IR Reflow Test System Operation Instruction
- **Greatek Spec #QA-00-304** Solderability Test Operation Instruction
- **Greatek Spec #QA-00-305** Temperature cycling
- **Greatek Spec #QA-00-402** SAT Operation Instruction

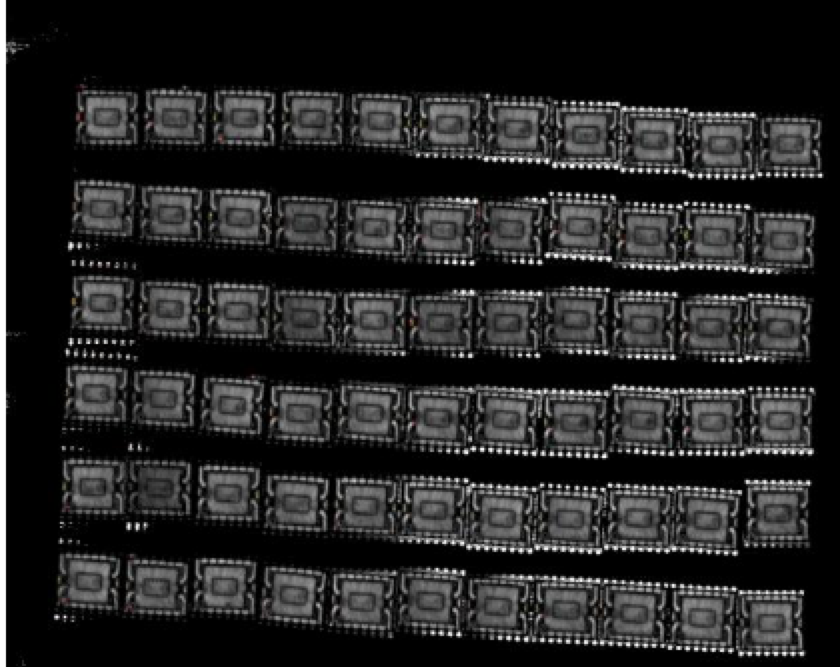
No.136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien Taiwan R.O.C.
Tel : (037)638-568 Fax : (037)628-323

8. Attachments:

IR PROFILE(Tmax:260℃) for SMD.

9. SAT Photo :

9.1 Before / After Precondition :



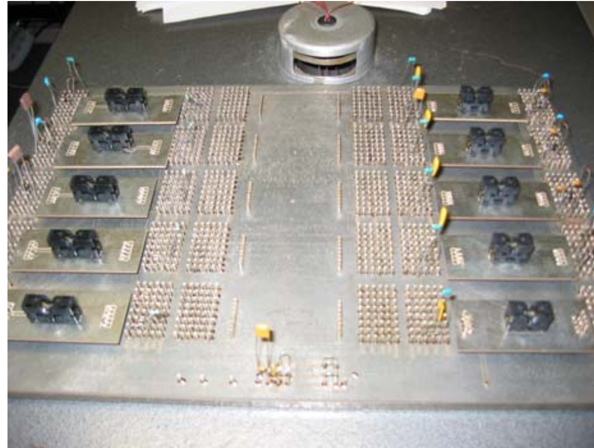
Package Type: TSSOP 16L
Before Pre-con LEVEL 3
Photo no : Fig 1
Comment : Focus on Die Surface SAT Result : 0/66ea PASS

Package Type: TSSOP 16L
After Pre-con LEVEL 3
Photo no : Fig 2
Comment : Focus on Die Surface SAT Result : 0/66ea PASS

Appendix II

Testing Equipment

Burn-in board and burn-in quipment



Burn-in Board used for testing

Burn-in oven used for testing

ESD Testing Equipment

Front view of the iMCS model #700

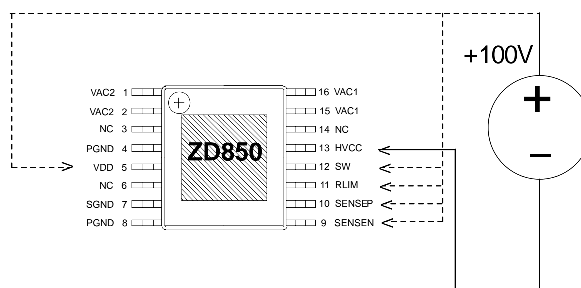
Front view of the iMCS model #700 with lid open

Back view of the ESD Tester with the Machine Model/Pulse Model being used

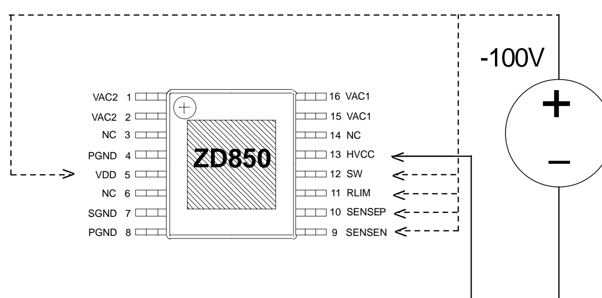
Appendix III

ESD Test Sequence for 16-TSSOP

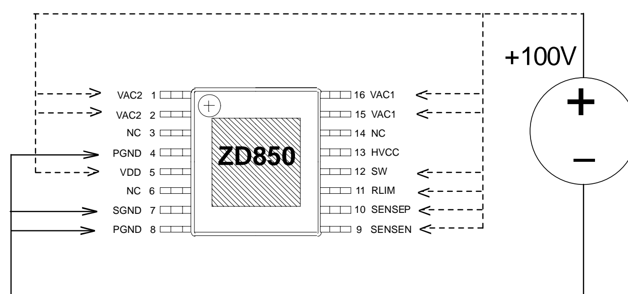
Step 1. Connect HVCC to ground and apply +100V to each pin, one at a time, except VAC+, VAC-, and the NC pins.



Step 2. Repeat Step 1 using -100V.



Step 3. Connect GND to ground and apply +100V to each pin, one at a time, except VAC+, VAC-, and the NC pins.



Step 4. Repeat Step 3 using -100V.
Step 5. Check DUT for damage.
Step 6. If DUT is undamaged, repeat Steps 1-5 for two additional units.
Step 7. When three units pass sequence, repeat Steps 1-6 for three additional parts and increase voltage by |100|V until |1000|V is reached and passed