



Reliability Qualification Report

ZD832 TransformerFree™ AC/DC LED Display Driver

Date: May 20, 2009
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Revision: 1.0

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Reliability Life Test Result

Life Test

Life Testing is performed to determine if device has any fundamental reliability related failure mechanisms, which can be divided into 4 main groups:

- Process or die related failures, such as oxide-related defects, metallization-related defects and diffusion-related defects.
- Assembly-related defects such as wire bonding or package-related failures.
- Design-related defects.
- Miscellaneous, undetermined or application-induced failures.

Life Test Result

Product Family:	TransformerFree™ AC/DC LED Display Driver
Device Type:	ZD832
Mask Sets:	MS182C
Processes:	Episil SOI 100V BiCMOS Process
Wafer Manufacturer:	Episil Technologies, Inc.
Package Type:	20-Pin Exposed TSSOP
Package Manufacturer:	Greatek Electronics Inc. in Taiwan
Die Attach Adhesive:	CRM-1033BF
Bond Wire:	Gold wire 1.2 mil
Test:	Refer to Reliability Test Results in Greatek's Reliability report
Reference Standard:	Mil-Std-883
Pass/Fail Criteria:	Electrical QA testing to datasheet limits at 25°C before and after stress.

Summary:

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD832LEY	500hr @ 120VAC	B6A19544H.T	10/5/2007	95	20	0

Device Type	HTOL Test	Lot Number	Date Completed	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD832LEY	500hr @ 120VAC	B6A19544H.T	11/6/2007	125	20	0
ZD832LEY	1000hr @ 120VAC	B6A19544H.T	11/27/2007	125	20	0

Device Type	HTOL Test	Lot Number	Target Date	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD832LEY	500hr @ 120VAC	B7921N56A.T	3/28/2008	125	20	
ZD832LEY	1000hr @ 120VAC	B7921N56A.T	4/18/2008	125	20	

Device Type	HTOL Test	Lot Number	Target Date	Burn-In Temperature (°C)	Sample Size	No. of Fails
ZD832LEY	500hr @ 220VAC	B7921N56A.T	3/28/2008	125	20	
ZD832LEY	1000hr @ 220VAC	B7921N56A.T	4/18/2008	125	20	

FIT Rate Calculation

The FIT (failures in time) is calculated as follows,

$$\text{FR (Chi-squared)} = \chi^2_{2n+2} / (2 \times \text{AF} \times \text{device-hours}) \times 10^9$$

where AF is the acceleration factor and n is the number of failures. The value is highly dependent on the following:

1. Life test conditions (duration, temperature, sample size and number of failures)
2. Activation energy of the potential failure modes

The weighted activation energy, E_a , of observed failure mechanisms of Zywyn products has been determined to be 0.8eV.

Based on the above criteria, the FIT rates at 25°C, 55°C, and 75°C operation at both 60% and 90% confidence levels for the ZD832 using Episil SOI 100V BiCMOS Process have been calculated and are listed below.

Device Type	Confidence Level	+25°C	+55°C	+75°C
ZD832	60%	18.67	319.88	1619.8
ZD832	90%	46.91	803.85	4070.46

1 FIT = 1 failure per billion device hours

ESD Test Results

ZD832 devices were submitted for Human Body Model ESD test.

Summary:

Device Type	ESD Test	Lot Number	Date Completed	Sample Size	No. of Fails
ZD832LEY	±2000V HBM	B6A19544H.T	2/14/2008	10	0

Temp Cycle Test Result

Zywyn's TransformerFree™ AC/DC LED driver products are packaged in a 20-Pin Exposed TSSOP Green Package. The packaged device Qualification Reliability Report which consists of Temp Cycle Test from vendors, is attached for reference. The report shows the devices pass the test with no failure.

Appendix I

20-PIN Exposed & 24-PIN Exposed TSSOP Reliability Report



GREATEK ELECTRONICS INC.

No.136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien Taiwan R.O.C.

Tel : (037)638-568 Fax : (037)628-323

Reliability Test Report

Customer : Zywyn Corporation

Purpose : New Package Qual Reliability Test

Package Type : TSSP 20L & TSSP 24L

Report No : B510-RELI-0708001

Report Date : 22-OCT-2007

Conclusion : The test results were all passed

Approved By: STEVEN SL Prepared By: Wanda Wei

Date : 22-OCT-2007

Date : 22-OCT-2007

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GREATEK ELECTRONICS INC.

No.136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien Taiwan R.O.C.

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1. Sample Background

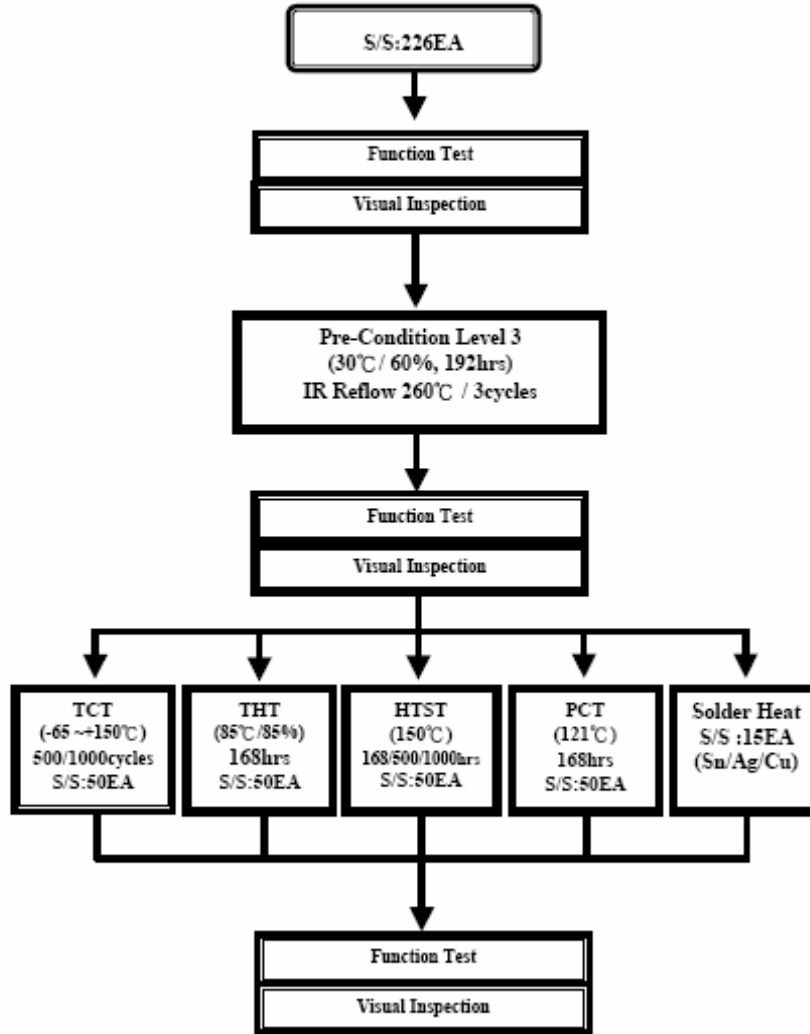
1.1 Sample Background:

Package Type :	TSSOP 24L	Lead Frame:	112*18E (mil)
Device :	*	Silver Epoxy:	8352L
Lot No:	*	Gold Wire:	1.5mil
Mo No:	UBA24U674139	Compound	G600F
Coating :	NO	Lead Finish	Pure Tin
Apply Date:	04-AUG-2007	Sample Size:	241EA
Complete Date:	23-SEP-2007	Report No:	B510-RELI-0708001



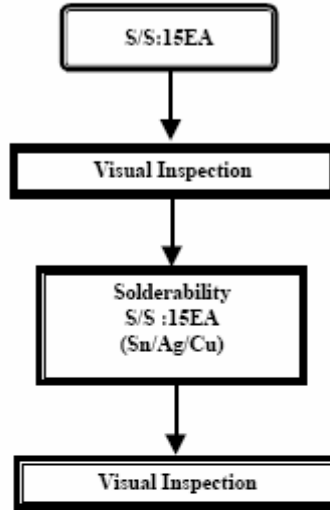
2. Test Flow Chart

2.1 Precondition:





2.2 Solderability:





3. Inspection method

3.1 Visual Inspection:

Purpose: In order to check whether the samples have package crack or not before/after reliability test.

Apparatus: Power Scope (7~40x)

3.2 SAT Inspection:

Purpose: Inspecting the delamination of concerned layer.

Apparatus: SONIX QUANTUM-350

4. Environment Stress / Mechanical Test

4.1 Precondition:

This test method establishes an industry standard preconditioning flow for plastic SMDs (surface mount device) that is representative of a typical industry multiple solder reflow operation.

Test procedure is as following:

Step1: TCT 5cycles

Step2: Bake 125°C ,24hrs

Step3: Moisture Soak (30°C/60%/192hrs)

Step4: IR Reflow 260°C / 3cycles

4.2 PCT:

The "Accelerated Moisture Resistance Test" is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged solid state devices. It employs severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. This test is destructive; it may* be used for qualification, lot acceptance and as a product monitor.

Test condition: 121°C , 2atm, 168hrs.

4.3 TCT:

This test is conducted to determine the resistance of a part to extremes of high- and low-temperatures, and to the effect of alternate exposures to these extremes.

Test condition: -65°C ~ 150°C ,500/1000cycles.

4.4 HTST:

The purpose of this test is to determine the effect on solid state electronic devices of storage at elevated temperature without electrical stress applied. This test is considered destructive and, therefore, is applicable for device qualification.

Test condition: 150°C , 168/500/1000hrs



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4.5 THT(egual to THB without bias):

The Steady-State Temperature Humidity Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs conditions of temperature and humidity which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Test condition: 85°C/85%,168hrs

4.6 Solderability:

The purpose of this test method is to evaluation the solderability of terminations that are normally joined by soldering operation. This evaluation is made on the basis of the ability of these terminations be wetted by a coating of solder ,and to produce a suitable fillet when dip soldered.

Test procedure is as following:

Step1: Steam aging (8hrs)

Step2: Dipping with flux(type R) , Condition: 245±5°C , Dwell Time:5±0.5secs.

4.7 Solder Heat:

The purpose of this test method is to evaluation the solderability of terminations that are normally joined by soldering operation. This evaluation is made on the basis of the ability of these terminations be wetted by a coating of solder ,and to produce a suitable fillet when dip soldered.

Test procedure is as following:

Step1: Condition: 260°C , Dwell Time:10secs.

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5. Reliability Test Results

5.1 Summary of test results:

Test Procedure	Sample Size	Visual Insp. Rej/s.s	Function Test rej/s.s	SAT insp Rej/s.s	Judgment
Before Pre-condition	226EA	0/226	0/226	0/11	PASS
After Pre-condition	226EA	0/226	0/226	0/11	PASS
PCT 168hrs	50EA	0/50	0/50	N/A	PASS
THT 168hrs	50EA	0/50	0/50	N/A	PASS
HTST 168hrs	50EA	0/50	0/50	N/A	PASS
HTST 500hrs	50EA	0/50	0/50	N/A	PASS
HTST 1000hrs	50EA	0/50	0/50	N/A	PASS
TCT 500cycles	50EA	0/50	0/50	N/A	PASS
TCT 1000cycles	50EA	0/50	0/50	N/A	PASS
Solder Heat	15EA	0/15	0/15	N/A	PASS
Solderability	15EA	0/15	N/A	N/A	PASS

5.2 Detail Informations of SAT Inspection :

Focus	Die Surface (Top)				Die Pad(back side)			
	0% acc	0%~10% rej	>10% rej	SAT Photo	0%	0%~50% acc	>50% rej	SAT Photo
Before Precondition	11	0	0	Fig-1	Exposed pad			
After Precondition	11	0	0	Fig-2	Exposed pad			

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6. Conclusion

6.1 The test results were all passed.

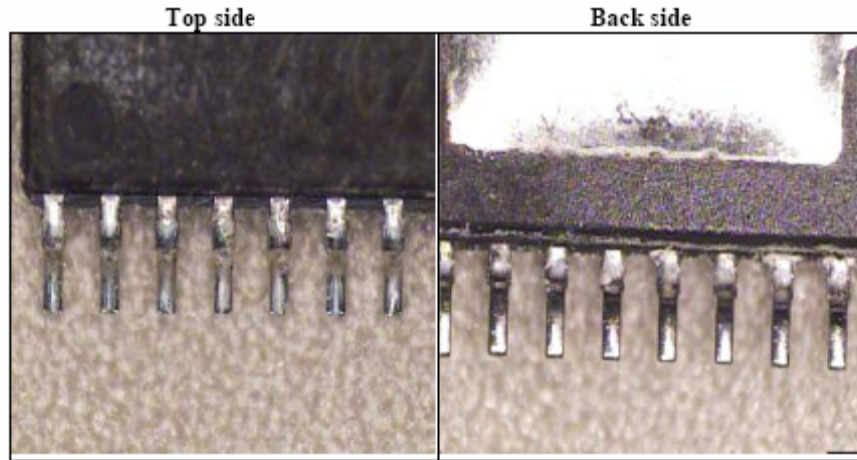
7. Reference

- * JESD22-A113 Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing
- * Greatek Spec #QA-00-300 Reliability Test Instruction
- * Greatek Spec #QA-00-301 Pressure Cooker Test
- * Greatek Spec #QA-00-302 Temperature/Humidity Chamber Operation Instruction
- * Greatek Spec #QA-00-303 IR Reflow Test System Operation Instruction
- * Greatek Spec #QA-00-304 Solderability Test Operation Instruction
- * Greatek Spec #QA-00-305 Temperature cycling
- * Greatek Spec #QA-00-402 SAT Operation Instruction



8. Solder Picture:

8.1 After solderability :





9. Attachments:

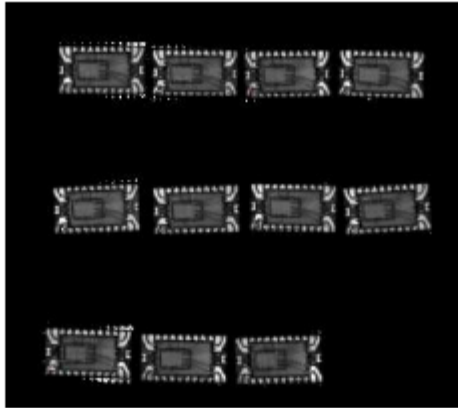
IR PROFILE(Tmax:260°C) for SMD.



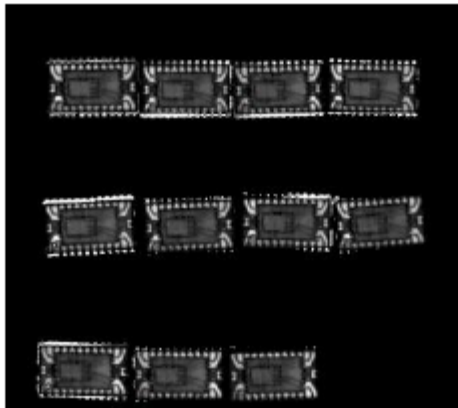


10. SAT Photo :

10.1 Before / After Precondition :



Package Type: TSSOP 24L
Before Pre-con Level 3
Photo no : Fig 1
Die Surface SAT Result : 0/11ea PASS

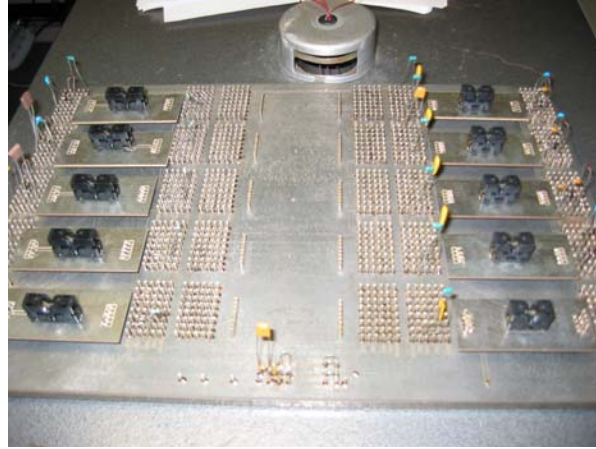


Package Type: TSSOP 24L
After Pre-con Level 3
Photo no : Fig 2
Die Surface SAT Result : 0/11ea PASS

Appendix II

Testing Equipment

Burn-in board and burn-in quipment



Burn-in Board used for testing



Burn-in oven used for testing

ESD Testing Equipment



Front view of the iMCS model #700



Front view of the iMCS model #700 with lid open

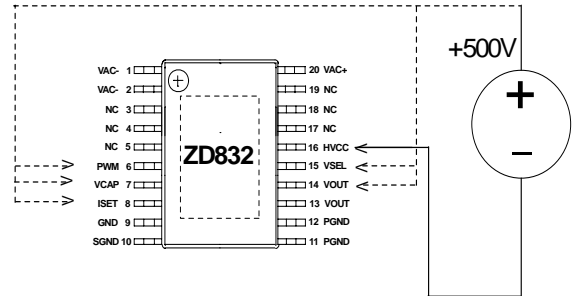


Back view of the ESD Tester with the Machine Model/Pulse Model being used

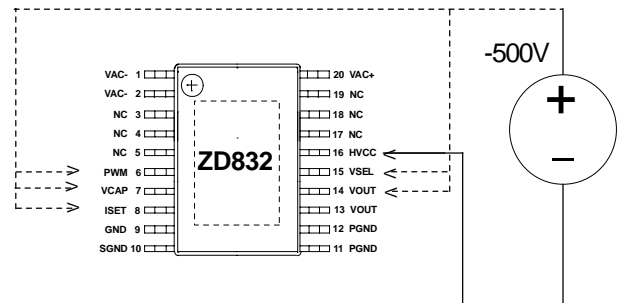
Appendix III

ESD Test Sequence for 20-EP-TSSOP

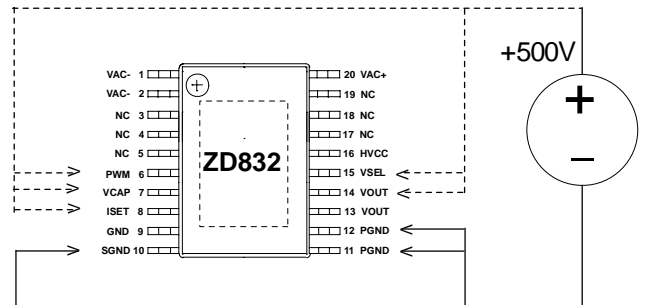
Step 1. Connect HVCC to ground and apply +500V to each pin, one at a time, except VAC+, VAC-, and the NC pins.



Step 2. Repeat Step 1 using -500V.



Step 3. Connect GND to ground and apply +500V to each pin, one at a time, except VAC+, VAC-, and the NC pins.



Step 4. Repeat Step 3 using -500V.

Step 5. Check DUT for damage.

Step 6. If DUT is undamaged, repeat Steps 1-5 for two additional units.

Step 7. When three units pass sequence, repeat Steps 1-6 for three additional parts and increase voltage by |500|V until |2000|V is reached and passed

